

CMOS EPL Series 20 A/B

RICOH EPL Series 20A/B are field-programmable logic arrays made possible by CMOS EPROM process technology.

Two product groups make up the EPL Series 20 A/B family.

Group I consists of AND-FIXED OR, XOR arrays, (EPL 10P8, 12P6, 14P4, and 16P2) available in 55ns or 35ns versions.

Group II consists of AND-FIXED OR, XOR array (EPL 16P8) and three Registered AND-FIXED OR, XOR arrays (EPL 16RP8, 16RP6, and 16RP4).

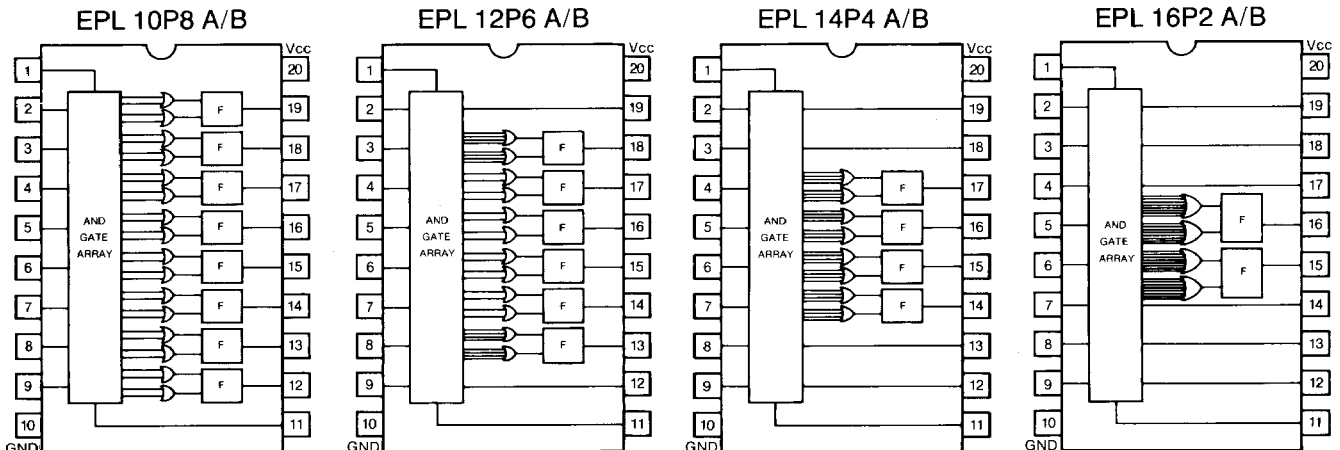
EPL Series 20A/B devices allow users to program by writing into EPROM Memory Cells. Series 20A/B are available in both one-shot plastic packages and reprogrammable Cerdip window packages.

Therefore, it is possible to shorten the development time and check and correct the circuits easily.

Features

- CMOS process technology ensures low power consumption and higher reliability
- Available in both Plastic and Cerdip window packages
- Data copying protection
- Flexibility of logic structure
- Package Type: 20-pin 300 mil Plastic DIP (one-shot)
20-pin 300 mil Ceramic DIP with a window (reprogrammable)
- Product Term: 32 (Group I)
64 (Group II)
- Propagation Delay Time:
55ns (max): Series 20 A
35ns (max): Series 20 B
- Each pin has programmable output polarity
- Upward compatibility with MMI devices, PAL™

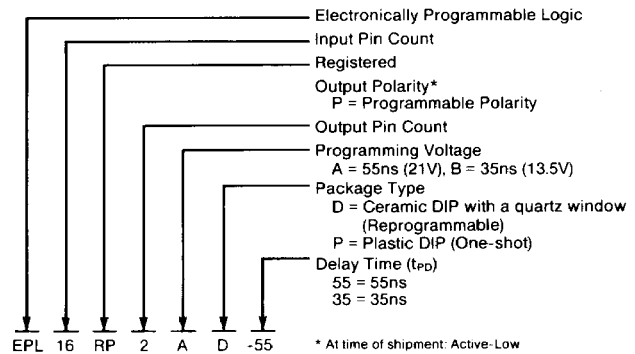
Logic Outlines Group I



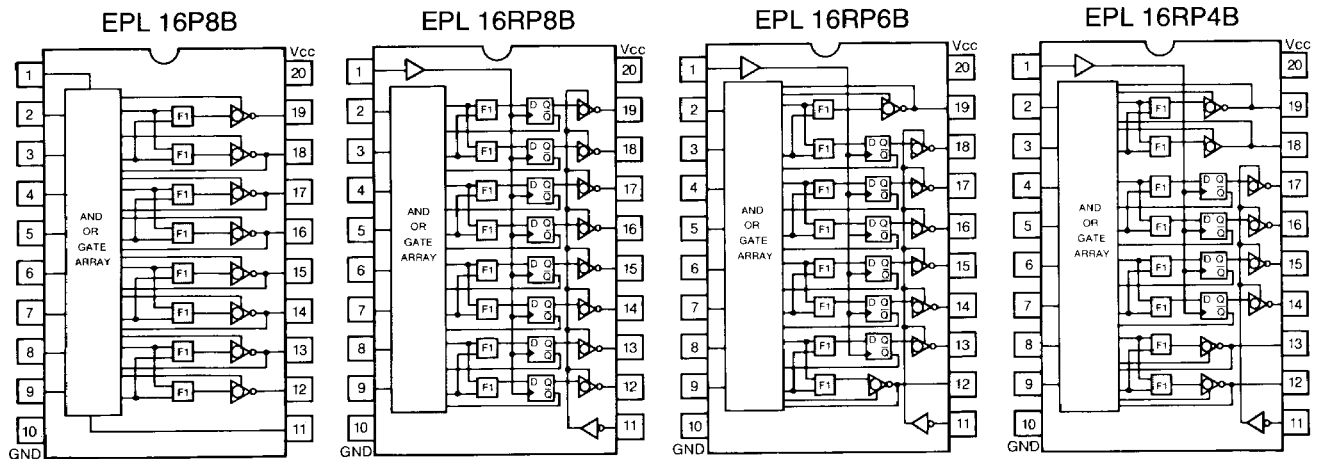
EPL Series 20 A/B Family

| Part Number | Configuration |
|-------------|--|
| 996291 | EPL 10P8 ✓ 10-Input, 8-Output, AND-OR, XOR array |
| 996292 | EPL 12P6 ✓ 12-Input, 6-Output, AND-OR, XOR array |
| 996293 | EPL 14P4 ✓ 14-Input, 4-Output, AND-OR, XOR array |
| 996294 | EPL 16P2 ✓ 16-Input, 2-Output, AND-OR, XOR array |
| 996295 | EPL 16P8 ✓ 10-Input, 6-I/O, 8-Output AND-OR, XOR array |
| 996296 | EPL 16RP8 ✓ 8-Input, 8-Feedback, 8-Output, 8-Registered AND-OR, XOR array |
| 996297 | EPL 16RP6 ✓ 8-Input, 6-Feedback, 2-I/O, 6-Output, 6-Registered AND-OR, XOR array |
| 996298 | EPL 16RP4 ✓ 16-Input, 8-Input, 4-Feedback, 4-I/O, 4-Output, 4-Registered AND-OR, XOR array |

Part Numbering System



Group II



NOTE: F - Feature Cell (OR, XOR, Polarity)

F1 - Feature1 Cell (OR, XOR)

Feature2 Cell (Polarity)

Electrical Specifications
Absolute Maximum Ratings

| Symbol | Item | Condition | Rated Value | Unit |
|------------------|--------------------------------|-----------------------|------------------------------------|------|
| V _{CC} | V _{CC} supply voltage | With respect to GND | -0.3 to 7 | V |
| V _{PP} | V _{PP} supply voltage | | A = -0.3 to 22.0, B = -0.3 to 14.5 | V |
| V _I | Input voltage | | -0.3 to V _{CC} = +0.3 | V |
| V _O | Output voltage | | -0.3 to V _{CC} = +0.3 | V |
| P _D | Max. power consumption | T _a = 25°C | 700 | mW |
| T _{OPR} | Ambient operating temperature | | 0 to 70 | °C |
| T _{STG} | Storage temperature | | -40 to 125 | °C |

EPL Series 20A D.C. Characteristics (T_a = 0 to 70°C, V_{CC} = 5V ± 5%)

| Symbol | Item | Condition | Min. | Typ. | Max. | Unit |
|------------------|-------------------------|--|------|------|-----------------------|------|
| I _{LI} | Input current leakage | V _{IN} = 0V to V _{CC} | -20 | | 20 | μA |
| V _{IL} | "L" input voltage | | -0.3 | | 0.8 | V |
| V _{IH} | "H" input voltage | | 2.0 | | V _{CC} + 0.3 | V |
| V _{OL} | "L" output voltage | V _{CC} = MIN, I _{OL} = 8mA* | | 0.3 | 0.5 | V |
| V _{OH} | "H" output voltage | V _{CC} = MIN, I _{OH} = 3.2mA* | 2.4 | 4.4 | | V |
| I _{CC1} | Supply current (Static) | Group I V _{CC} = MAX, Output = open V _I = GND or V _{CC} * | | 5.5 | 25 | mA |
| | | | | | 35 | mA |
| I _{CC2} | Supply current (Active) | Group I V _{CC} = MAX, Output = open f = 10MHz, V _I = 0.8V or 2.4V* | | 8 | 45 | mA |

EPL Series 20B D.C. Characteristics (Ta = 0 to 70°C, Vcc = 5V ± 5%)

| Symbol | Item | Condition | Min. | Typ. | Max. | Unit | |
|------------------|--------------------------------------|--|---|------|-----------------------|------|----|
| I _{LI} | Input current leakage | V _{IN} = 0V to V _{CC} | -20 | | 20 | μA | |
| V _{IL} | "L" input voltage | | -0.3 | | 0.8 | V | |
| V _{IH} | "H" input voltage | | 2.0 | | V _{CC} + 0.3 | V | |
| V _{OL} | "L" output voltage | V _{CC} = MIN, I _{OL} = 8mA** | | 0.3 | 0.5 | V | |
| V _{OH} | "H" output voltage | V _{CC} = MIN, I _{OH} = 3.2mA** | 2.4 | 4.4 | | V | |
| I _{LO} | Output current leakage in OFF status | Vo = 0V to Vcc | -20 | | 20 | μA | |
| I _{CC1} | Supply current (Static) | Group I | V _{CC} = MAX, Output open V _I = GND or V _{CC} * | | 10 | 40 | mA |
| | | | V _{CC} = MAX, Output = open V _I = 2.4V | | | 50 | mA |
| | | Group II | V _{CC} = MAX, Output = open V _I = GND or V _{CC} * | | 35 | 60 | mA |
| | | | V _{CC} = MAX, Output = open V _I = 2.4V | | | 70 | mA |
| I _{CC2} | Supply current (Active) | Group I | V _{CC} = MAX, Output = open | | 15 | 60 | mA |
| | | Group II | f = 10MHz, V _I = 0.8V or 2.4V* | | 40 | 80 | mA |

NOTES: Group I devices are equipped with power-down circuits. When neither "OR" nor "XOR" in the FEATURE cell is used, current for the unused product term is cut off. (Above mentioned specifications are conditional on the use of all product terms.)

*Typical I_{CC} values are for V_{CC} = 5.0V, 50% product term usage, Ta = 25°C

**Typical V_{OL} = 0.5V for I_{OL} = 16mA, Ta = 25°C

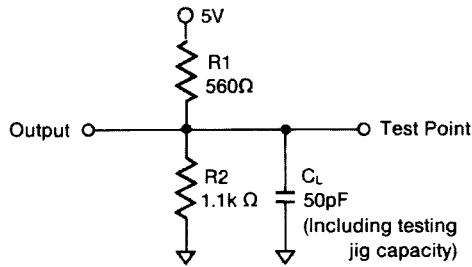
EPL Series 20A A.C. Characteristics (Ta = 0 to 70°C, Vcc = 5V ± 5%)

| Symbol | Item | Condition | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|---|------|------|------|------|
| t _{PD} | Input or feedback to output | R ₁ = 560Ω | | 45 | 55 | ns |
| f _{MAX} | Max. frequency | R ₂ = 1.1KΩ C _L = 50pF | | | 16 | MHz |

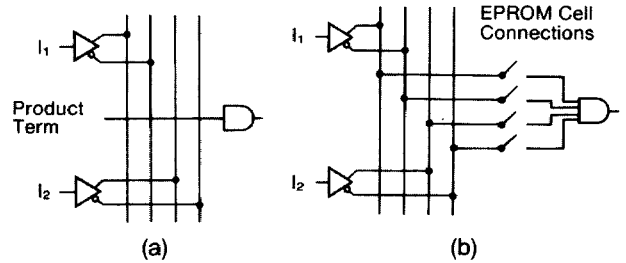
EPL Series 20B A.C. Characteristics (Ta = 0 to 70°C, Vcc = 5V ± 5%)

| Symbol | Item | | Condition | Typical | | | Unit | |
|------------------|-----------------------------------|-----------------------------|--|---------|------|------|------|-----|
| | | | | Min. | Std. | Max. | | |
| t _{PD} | Propa- gation Delay Time | Input or feedback to output | R ₁ = 560Ω R ₂ = 1.1KΩ C _L = 50pF | | 25 | 35 | ns | |
| t _{CLK} | | Clock to output or feedback | | | 15 | 25 | ns | |
| t _{PZX} | | Pin11 to output enable | | | 15 | 25 | ns | |
| t _{PXZ} | | Pin11 to output disable | | | 15 | 25 | ns | |
| t _{PIZ} | | Input to output enable | | | 25 | 35 | ns | |
| t _{PIX} | | Input to output disable | | | 25 | 35 | ns | |
| f _{MAX} | | Max. frequency | | | | | 20 | MHz |
| t _{WL} | | Minimum clock time width | | Low | | 20 | | ns |
| t _{WH} | | | | High | | 20 | | ns |
| t _{SU} | Input set-up time | | | 25 | | ns | | |
| t _H | Input hold time | | | 0 | | ns | | |

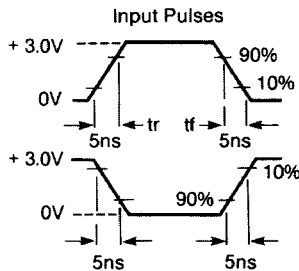
Output Load



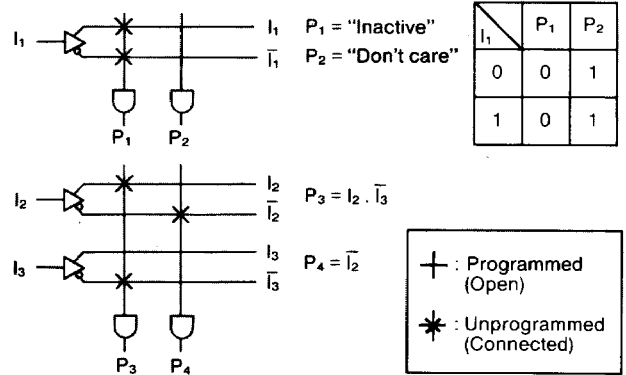
Logic Diagram



Input Waveform



NOTE: This is the A.C. characteristic measurement with a voltage of 1.5 V on both the input and output.



(c)

Configurations of EPL Logic

Ricoh EPL Series 20 A/B. Group I provides 32 input addresses and 32 product terms. Ricoh EPL Series 20 A/B Group II provides 32 input terms and 64 product terms. Input pins in both groups operate at TTL levels.

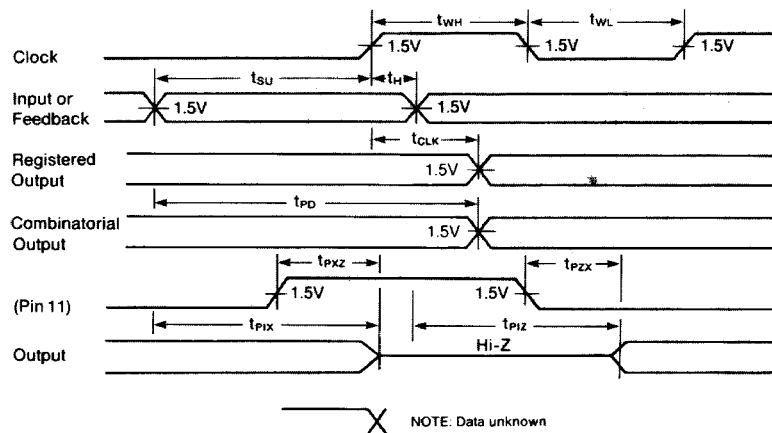
All intersection points of the input addresses and product terms are provided with an EPROM cell connection. These intersections are connected prior to delivery.

The AND gate is illustrated in logic diagram (a) above. The switches, indicated in logic diagram (b) correspond to the EPROM cell connections. All switches are closed when the devices are unprogrammed.

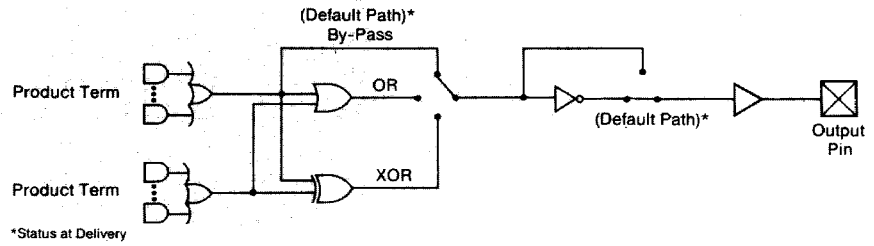
As illustrated in logic diagram (c), when neither positive input (I) nor negative input (I) is programmed, the AND output (P₁) becomes "inactive." When both positive input (I) and negative input (I) are programmed, the AND output (P₂) becomes "don't care" logically.

Each output includes a FEATURE cell in addition to the programmable AND-FIXED OR logic. The FEATURE cell enables the user to program the logic polarity (active-high/active-low) and the logical OR, Exclusive-OR case.

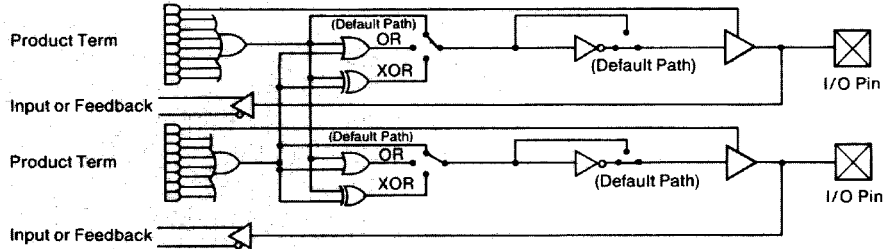
Timing Diagram



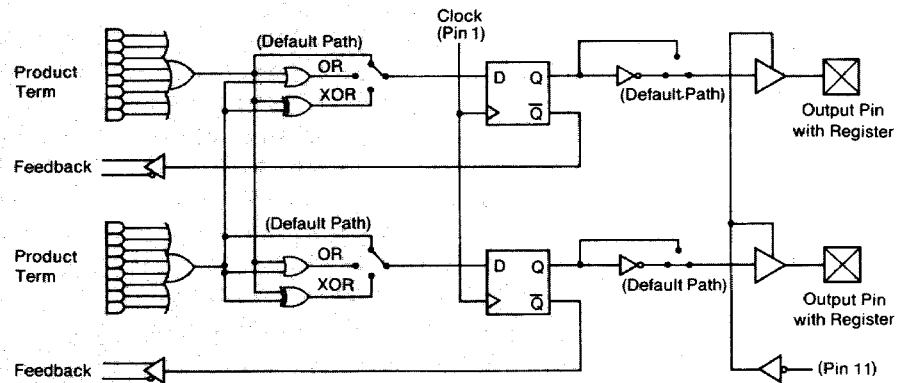
Group I
Block Diagram



Group II
I/O Block Diagram



Group II
Registered Block Diagram



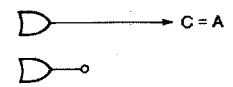
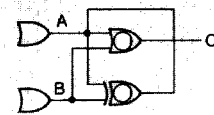
Feature Cell (MMI PAL and pin compatible)

Feature 1
OR/XOR

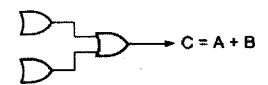
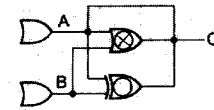
Unprogrammed State (MMI PAL pin compatible)

Unprogrammed State

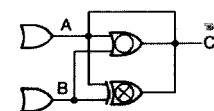
Final State



OR Program

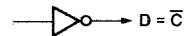


XOR Program



Feature 2
POLARITY

Unprogrammed State



POLARITY Program



Programming Modes

Ricoh EPL Series A/B go into the program/verify mode when Pin 1 (V_{PP}) has V_{IHP} (20A : 21V, 20B : 13.5V) applied.

Two program/verify modes exist to program/verify the AND array and to program/verify the FEATURE CELL.

| AND Array | Programming | Verification |
|--------------------------------|---|--|
| (See AND Array Timing Diagram) | <ul style="list-style-type: none"> ■ Apply V_{IHP} (20A : 21V, 20B : 13.5V) to Pin 1 (V_{PP}) ■ Set Address A0-A7 ■ Set Data D0-D7 Data "L" is programmed Data "H" is not programmed ■ Execute program by applying each 1ms pulse of V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 11 (PGM/OE), as illustrated in following flow chart | <ul style="list-style-type: none"> ■ Apply V_{IHP} (20A : 21V, 20B : 13.5V) to Pin 1 (V_{PP}) ■ Set Address A0-A7 ■ Verify Data D0-D7 with Pin 11 (PGM/OE) set to V_{IL} |

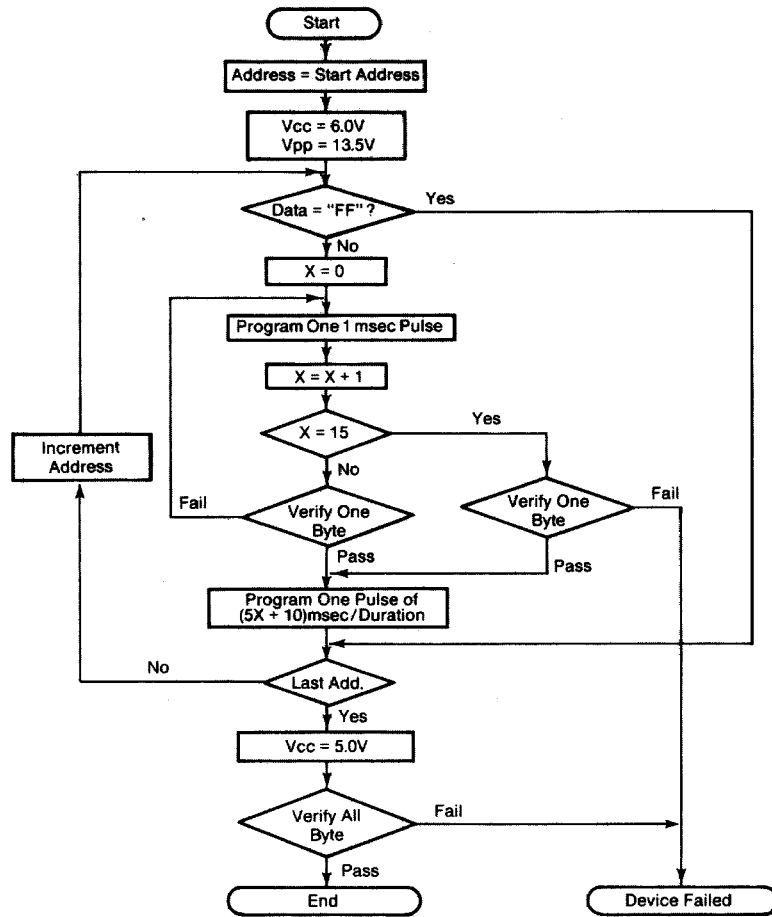
| Feature Cell | Programming | Verification |
|--------------|--|--|
| | <ul style="list-style-type: none"> ■ Apply V_{IHP} (20A : 21V, 20B : 13.5V) to Pin 1 (V_{PP}) ■ Apply V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 5 (FPM) ■ Select Feature Cell Attributes via Pin 3 (S1) and Pin 4 (S2) (See table 2) ■ Set Feature Cell Data Data "L" is programmed Data "H" is not programmed ■ Execute program by applying each 1ms pulse of V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 11 (PGM/OE) as illustrated in following flow chart | <ul style="list-style-type: none"> ■ Apply V_{IHP} (20A : 21V, 20B : 13.5V) to Pin 1 (V_{PP}) ■ Apply V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 5 (F_{PM}) ■ Select Feature Cell Attributes via Pin 3 (S1) and Pin 4 (S2) (See table 2) ■ Set Pin 11 (PGM/OE) to "V_{IL}" Level |

| Security Cell | Programming | Verification |
|---------------|---|--------------|
| | <ul style="list-style-type: none"> ■ Apply V_{IHP} (20A : 21V, 20B : 13.5V) to Pin 1 (U_{PP}) ■ Apply V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 5 (FPM) ■ Set "L" Level to Pin 12 (D0/Security) ■ Execute Security Program by applying 50ms pulse and V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 11 (PGM/OE) | |

Table 2

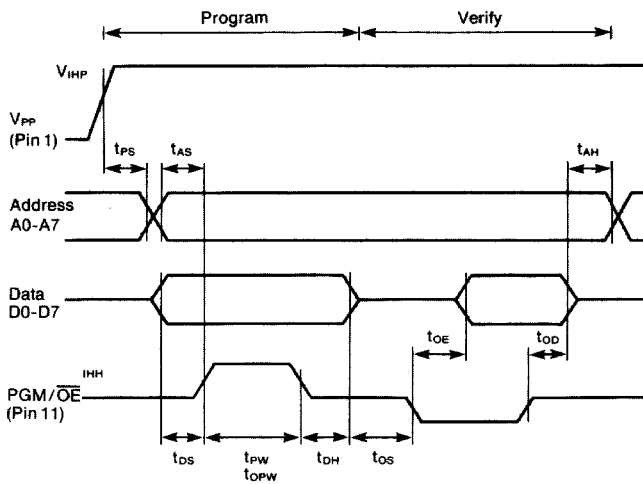
| S1 | S2 | Feature Cell |
|----|----|--------------|
| 0 | 0 | OR |
| 0 | 1 | XOR |
| 1 | 0 | Polarity |
| 1 | 1 | Security |

0 : V_{IL}
1 : V_{IH}

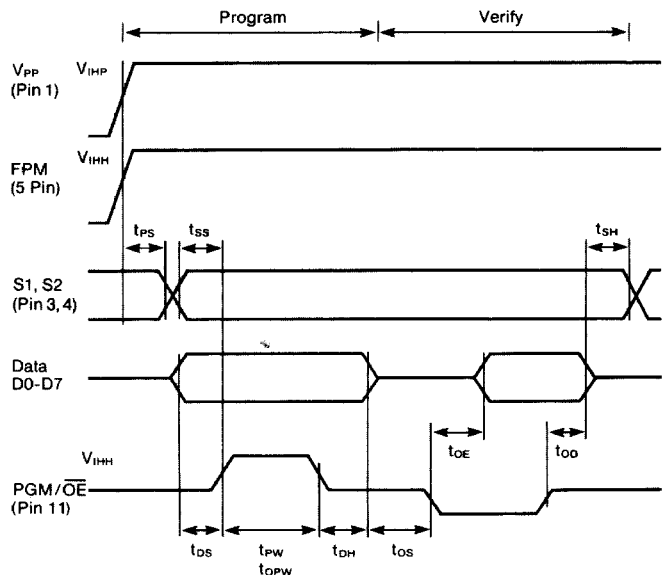


Timing Diagram

1. AND Array* Programming/Verification



2. Feature Cell* Programming/Verification

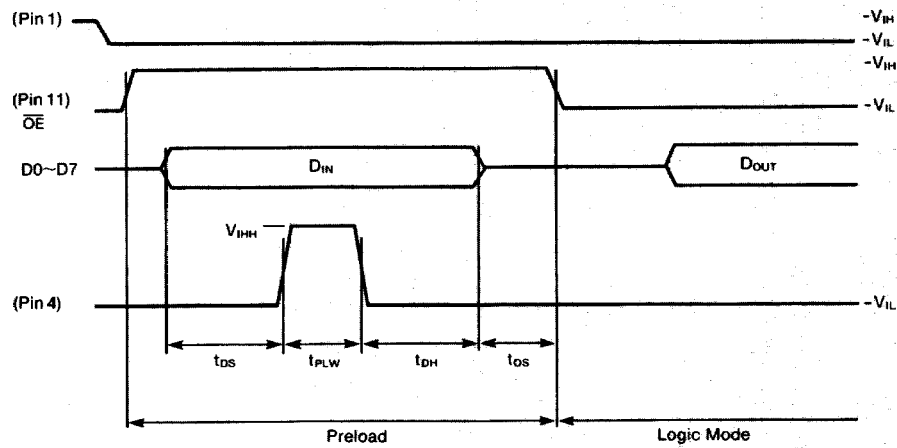


Preload Mode: EPL 16RP8, EPL 16RP6, EPL 16RP4

The data of each pin is preloaded to F/F with the steps in the table below.

| Preload Mode | Read |
|---|---|
| <ul style="list-style-type: none"> ■ Apply V_{IL} to Pin 1 (CLK) ■ Apply V_{IH} to Pin 11 (OE) ■ Set the preload data to the data pin ■ Apply the preload pulse of 2μs pulse width of V_{IHH} (20A : 15V, 20B : 13.5V) to Pin 4 (PRELOAD/S2/A5) | Same F/F Read operation as in normal logic mode |

Timing Diagram



Programming Electrical Specifications

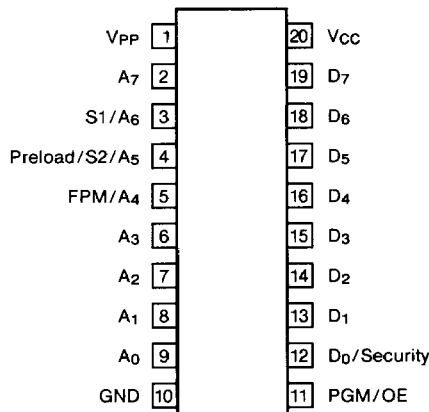
D.C. Attributes (TA = 20 ~ 30°C, Vcc = 6.0 ± 0.25V)

| Symbol | Item | Requirements | Typical | | | Unit |
|-----------|--|-------------------------|---------|------|----------------|---------|
| | | | Min. | Avg. | Max. | |
| I_{LI} | Input leakage current | $V_I = 0V \sim V_{CC}$ | -20 | | 20 | μA |
| I_{LO} | Output leakage current | $V_O = 0V \sim V_{CC}$ | -20 | | 20 | μA |
| V_{IL} | Input voltage "L" | | -0.3 | | 0.8 | V |
| V_{IH} | Input voltage "H" | | 2.5 | | $V_{CC} + 0.3$ | V |
| V_{IHH} | Programmed input voltage "H"-Series 20A | | 14.5 | 15.0 | 15.5 | V |
| V_{IHH} | Programmed input voltage "H"-Series 20B | | 13.0 | 13.5 | 14.0 | V |
| V_{IHP} | Programmed supply voltage-Series 20A | | 20.5 | 21.0 | 21.5 | V |
| V_{IHP} | Programmed supply voltage-Series 20B | | 13.0 | 13/5 | 14.0 | V |
| I_{HH} | Programmed power source current- V_{IHH} | $PGM/OE, FPM = V_{IHH}$ | | | 5 | mA |
| I_{HP} | Programmed power source current- V_{IHP} | $V_{PP} = V_{IHP}$ | | | 30 | mA |
| I_{CC} | Programmed power source current- V_{CC} | | | | 5 | mA |

A.C. Attributes (TA = 20 ~ 30°C, Vcc = 6.0 ± 0.25V)

| Symbol | Item | Min. | Avg. | Max. | Unit |
|------------------|------------------------------|-------|------|-------|------|
| t _{PS} | V _{IHP} set-up time | 2 | | | μS |
| t _{AS} | Address set-up time | 2 | | | μS |
| t _{DS} | Data set-up time | 2 | | | μS |
| t _{PW} | Program pulse width | 0.95 | 1.0 | 1.05 | mS |
| t _{DH} | Data hold time | 2 | | | μS |
| t _{OS} | OE set-up time | 2 | | | μS |
| t _{OE} | OE access time | | | 2 | μS |
| t _{OO} | Data effective time after OE | 0 | | 2 | μS |
| t _{AH} | Address hold time | 2 | | | μS |
| t _{SS} | Select set-up time | 2 | | | μS |
| t _{SH} | Select hold time | 2 | | | μS |
| t _{PLW} | Preload pulse width | 2 | | | μS |
| t _{OPW} | Over pulse width | 14.75 | | 88.75 | μS |

Pin Layout Diagram
Program Mode



Mode Table

| Pin Connection/Function Definitions | | | | | | | | | | | |
|-------------------------------------|--------------------------|----|----|----|----|----|----|----|----|----|-------------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 11 | 12-19 |
| AND Array Program | HP | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | HH | Data Input |
| AND Array Verify | HP | A7 | A6 | A5 | A | A3 | A2 | A1 | A0 | L | Data Output |
| Feature Program | HP | X | S1 | S2 | HH | X | X | X | X | HH | Data Input |
| Feature Verify | HP | X | S1 | S2 | HH | X | X | X | X | L | Data Output |
| Preload | L | X | X | HH | X | X | X | X | X | H | Data Input |
| Logic Mode | All Inputs are TTL Level | | | | | | | | | | |

NOTES: HP = V_{IHP} (Series 20A : 21V, Series 20B : 13.5V)
 HH = V_{IHH} (Series 20A : 15V, Series 20B : 13.5V)
 H = V_{IH}
 L = V_{IL}
 X = Don't care (TTL Level)

Programmer Support

| Manufacturer | Programmer | RICOH EPL Personality Module |
|----------------------|---------------------|--|
| Data I/O | Model 29B, Model 60 | Universal CMOS PAL Adapter 303A - 011A |
| Minato Electronics | Model 1870A | 7SP-REPL20 |
| Valley Data Sciences | 150/160 Series | None |
| Stag | ZL30 | None |
| Oliver | OMNI | None |

NOTE: Other programmer vendors to be announced.

Support Software

| Manufacturer | Name of Software | Operating System |
|---------------------|------------------|---|
| Data I/O | ABEL™ | MS-DOS™ DEC VAX/VMS™ DEC VAX/UNIX™ |
| Assisted Technology | CUPL™ | MS-DOS CP/M-86™ DEC VAX/VMS DEC VAX/UNIX |
| RICOH | EPLASM™ | MS-DOS VAX/VMS |

Address Table - Group I
Input Line No. vs. Address

| Input Line | Address Pin State | | | | |
|------------|-------------------|----|----|----|----|
| Number | A4 | A3 | A2 | A1 | A0 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 |
| 16 | 1 | 0 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 1 |
| 20 | 1 | 0 | 1 | 0 | 0 |
| 21 | 1 | 0 | 1 | 0 | 1 |
| 22 | 1 | 0 | 1 | 1 | 0 |
| 23 | 1 | 0 | 1 | 1 | 1 |
| 24 | 1 | 1 | 0 | 0 | 0 |
| 25 | 1 | 1 | 0 | 0 | 1 |
| 26 | 1 | 1 | 0 | 1 | 0 |
| 27 | 1 | 1 | 0 | 1 | 1 |
| 28 | 1 | 1 | 1 | 0 | 0 |
| 29 | 1 | 1 | 1 | 0 | 1 |
| 30 | 1 | 1 | 1 | 1 | 0 |
| 31 | 1 | 1 | 1 | 1 | 1 |

NOTES: 1. An unspecified input line will produce all low data.
2. (A7) Pin 2 must be at V_L for Group I EPLs.

Address Table - Group II
Input Line No. vs. Address

| Input Line | Address Pin State | | | | |
|------------|-------------------|----|----|----|----|
| Number | A4 | A3 | A2 | A1 | A0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |
| 2 | 0 | 0 | 0 | 0 | 1 |
| 3 | 0 | 0 | 0 | 0 | 0 |
| 4 | 1 | 1 | 1 | 0 | 1 |
| 5 | 1 | 1 | 1 | 0 | 0 |
| 6 | 0 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 | 0 |
| 8 | 1 | 1 | 0 | 1 | 1 |
| 9 | 1 | 1 | 0 | 1 | 0 |
| 10 | 0 | 0 | 1 | 0 | 1 |
| 11 | 0 | 0 | 1 | 0 | 0 |
| 12 | 1 | 1 | 0 | 0 | 1 |
| 13 | 1 | 1 | 0 | 0 | 0 |
| 14 | 0 | 0 | 1 | 1 | 1 |
| 15 | 0 | 0 | 1 | 1 | 0 |
| 16 | 1 | 0 | 1 | 1 | 1 |
| 17 | 1 | 0 | 1 | 1 | 0 |
| 18 | 0 | 1 | 0 | 0 | 1 |
| 19 | 0 | 1 | 0 | 0 | 0 |
| 20 | 1 | 0 | 1 | 0 | 1 |
| 21 | 1 | 0 | 1 | 0 | 0 |
| 22 | 0 | 1 | 0 | 1 | 1 |
| 23 | 0 | 1 | 0 | 1 | 0 |
| 24 | 1 | 0 | 0 | 1 | 1 |
| 25 | 1 | 0 | 0 | 1 | 0 |
| 26 | 0 | 1 | 1 | 0 | 1 |
| 27 | 0 | 1 | 1 | 0 | 0 |
| 28 | 1 | 0 | 0 | 0 | 1 |
| 29 | 1 | 0 | 0 | 0 | 0 |
| 30 | 0 | 1 | 1 | 1 | 1 |
| 31 | 0 | 1 | 1 | 1 | 0 |

Product Line No. vs. Address

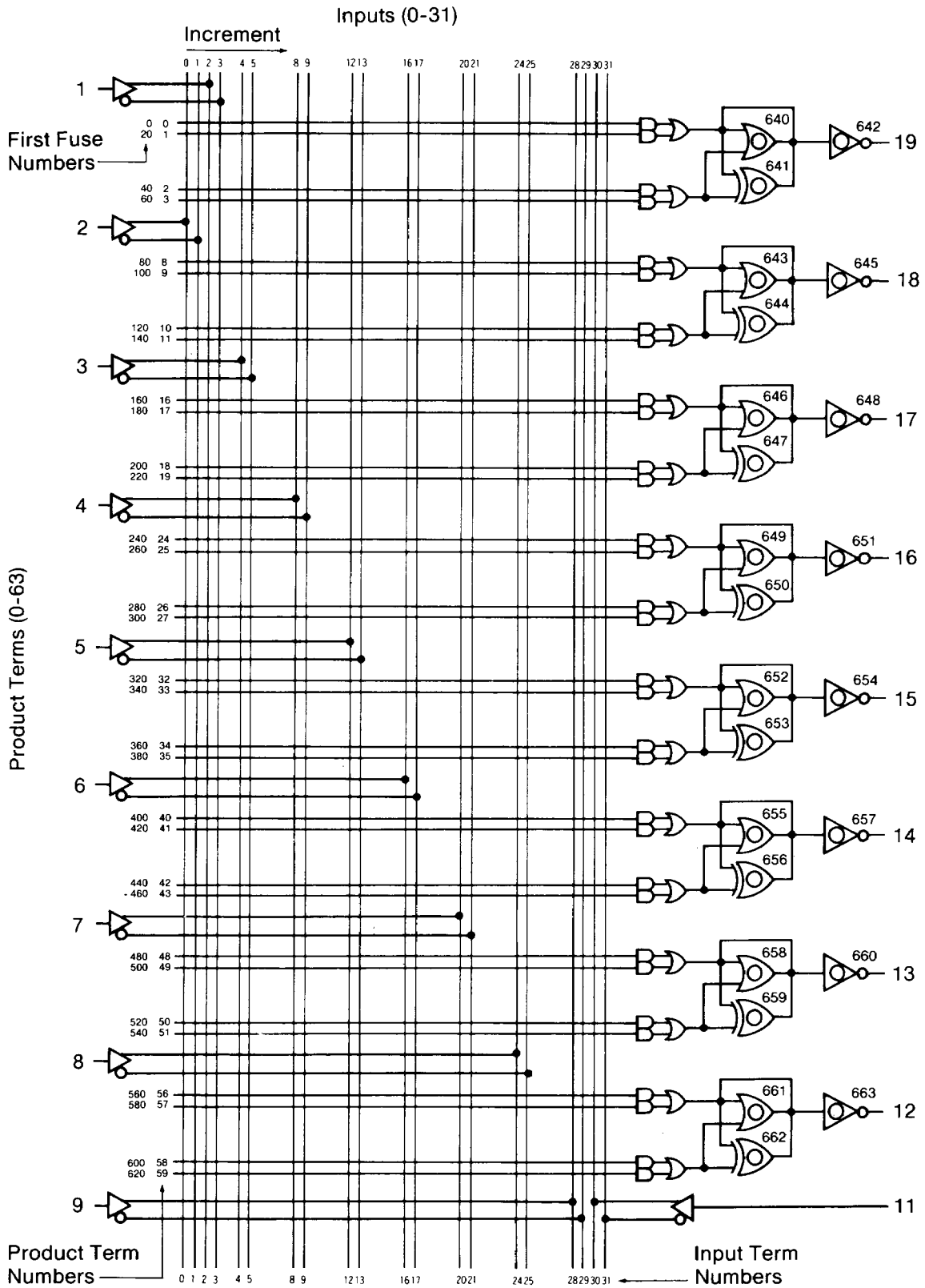
| Product Line Number | | | | | | | | Address Pin State | | |
|---------------------|----|----|----|----|----|----|----|-------------------|----|----|
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | A7 | A6 | A5 |
| 56 | 48 | 40 | 32 | 24 | 16 | 8 | 0 | 0 | 0 | 0 |
| 57 | 49 | 41 | 33 | 25 | 17 | 9 | 1 | 0 | 0 | 1 |
| 58 | 50 | 42 | 34 | 26 | 18 | 10 | 2 | 0 | 1 | 0 |
| 59 | 51 | 43 | 35 | 27 | 19 | 11 | 3 | 0 | 1 | 1 |
| 60 | 52 | 44 | 36 | 28 | 20 | 12 | 4 | 1 | 0 | 0 |
| 61 | 53 | 45 | 37 | 29 | 21 | 13 | 5 | 1 | 0 | 1 |
| 62 | 54 | 46 | 38 | 30 | 22 | 14 | 6 | 1 | 1 | 0 |
| 63 | 55 | 47 | 39 | 31 | 23 | 15 | 7 | 1 | 1 | 1 |

Product Line No. vs. Address

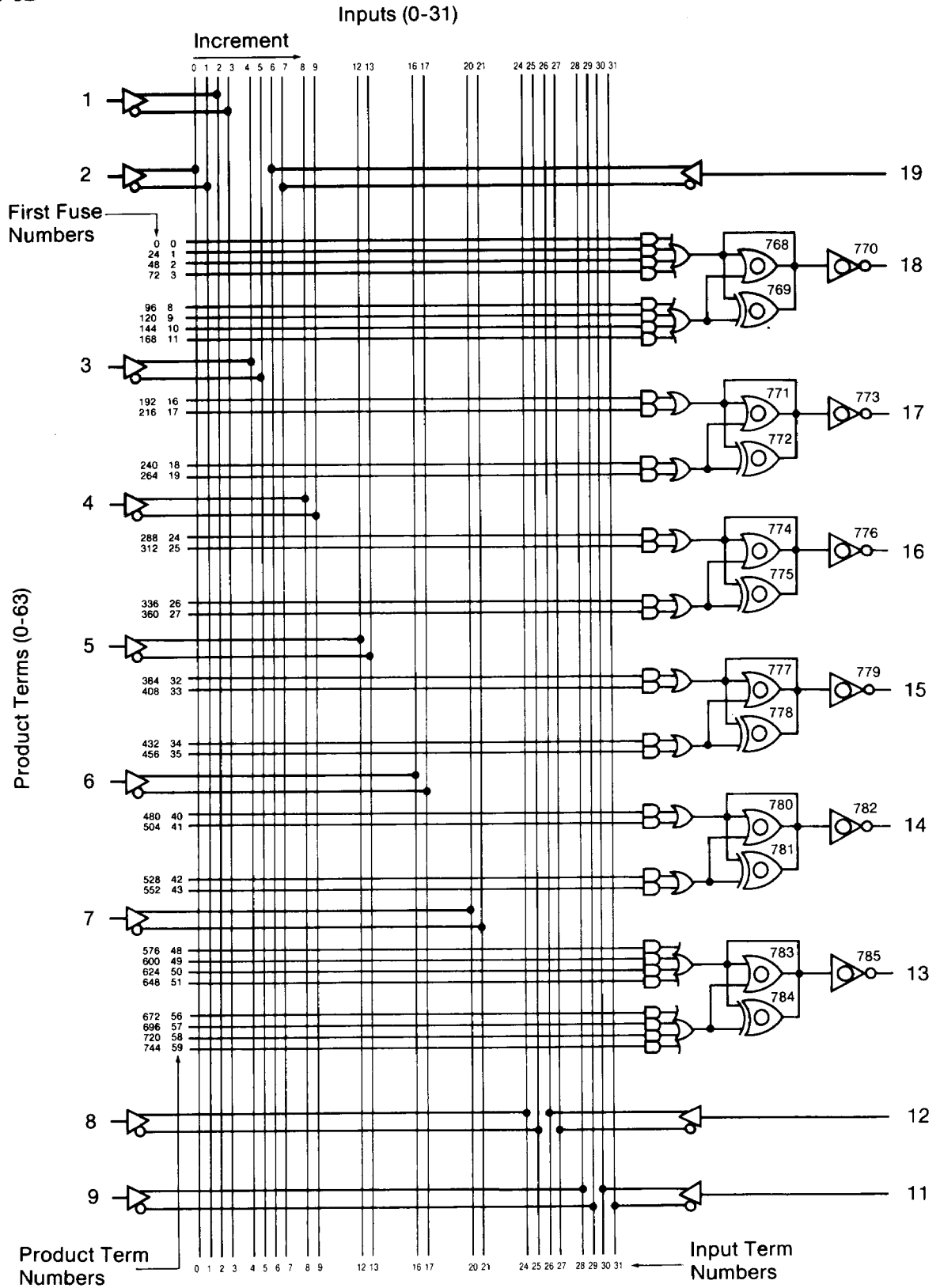
| Product Line Number | | | | | | | | Address Pin State | | |
|---------------------|----|----|----|----|----|----|----|-------------------|----|----|
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | A7 | A6 | A5 |
| 56 | 48 | 40 | 32 | 24 | 16 | 8 | 0 | 0 | 0 | 0 |
| 57 | 49 | 41 | 33 | 25 | 17 | 9 | 1 | 0 | 0 | 1 |
| 58 | 50 | 42 | 34 | 26 | 18 | 10 | 2 | 0 | 1 | 0 |
| 59 | 51 | 43 | 35 | 27 | 19 | 11 | 3 | 0 | 1 | 1 |
| 60 | 52 | 44 | 36 | 28 | 20 | 12 | 4 | 1 | 0 | 0 |
| 61 | 53 | 45 | 37 | 29 | 21 | 13 | 5 | 1 | 0 | 1 |
| 62 | 54 | 46 | 38 | 30 | 22 | 14 | 6 | 1 | 1 | 0 |
| 63 | 55 | 47 | 39 | 31 | 23 | 15 | 7 | 1 | 1 | 1 |

□ : Area not in use

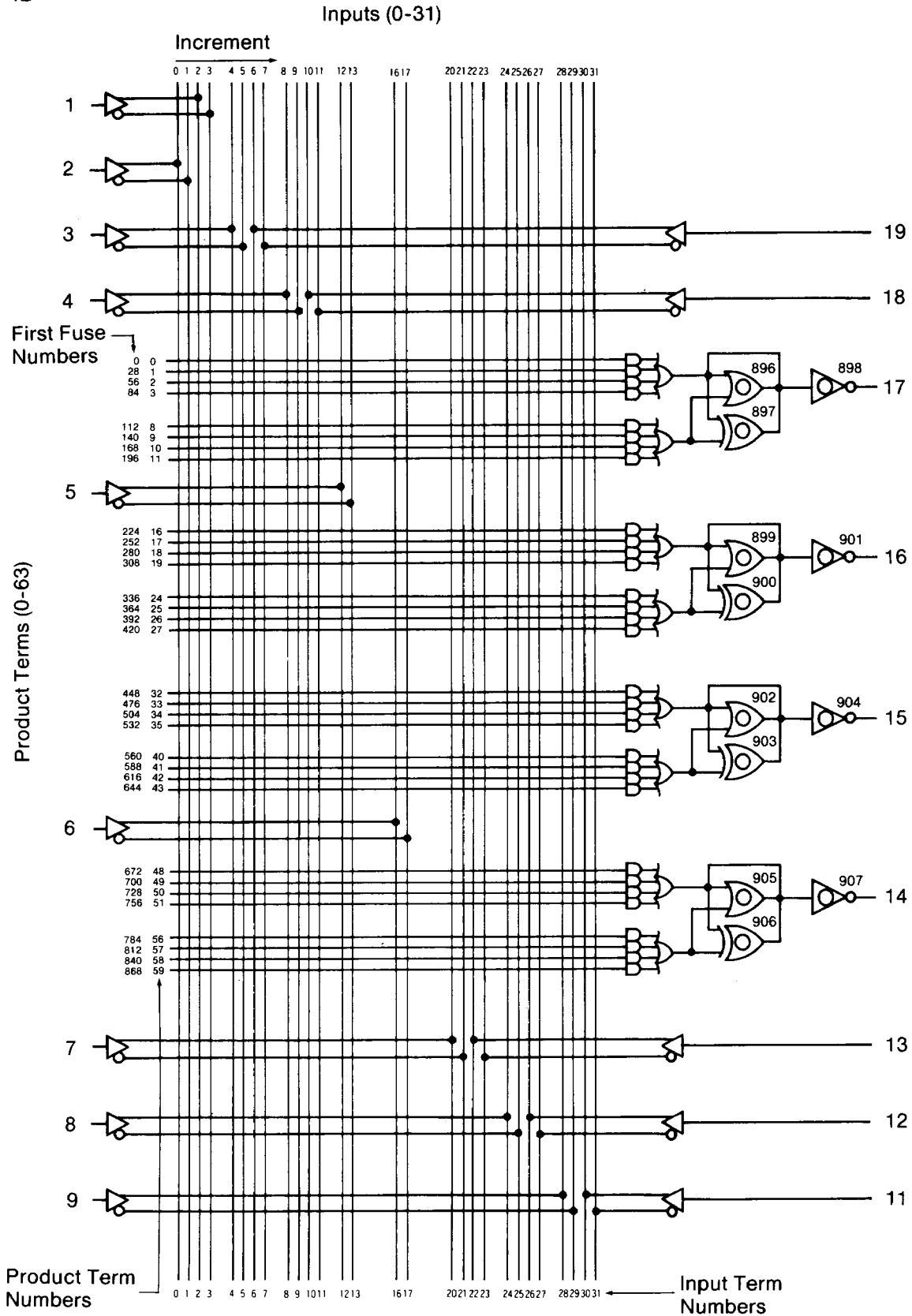
Logic Diagram
EPL10P8A
EPL10P8B



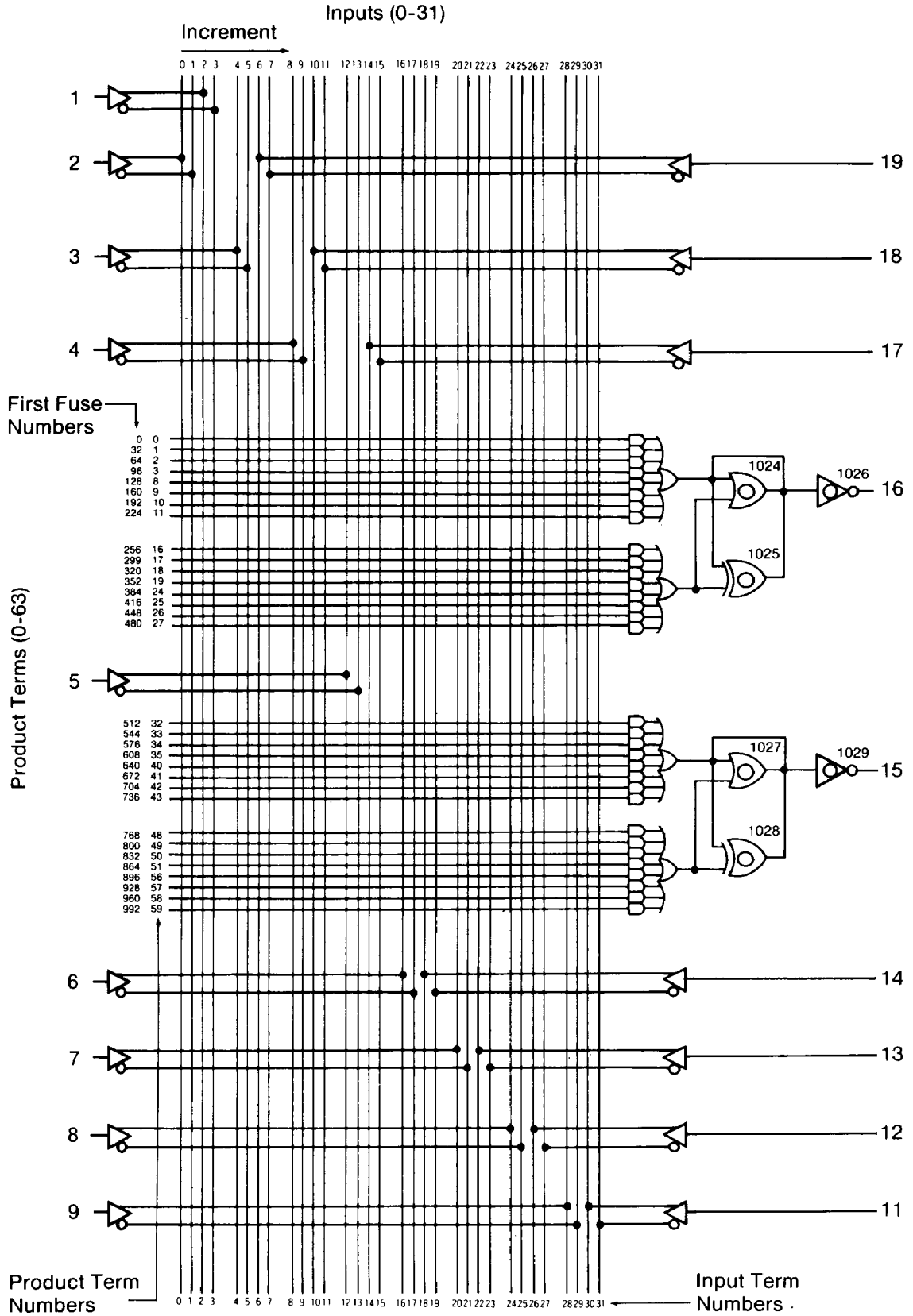
Logic Diagram
 EPL12P6A
 EPL12P6B



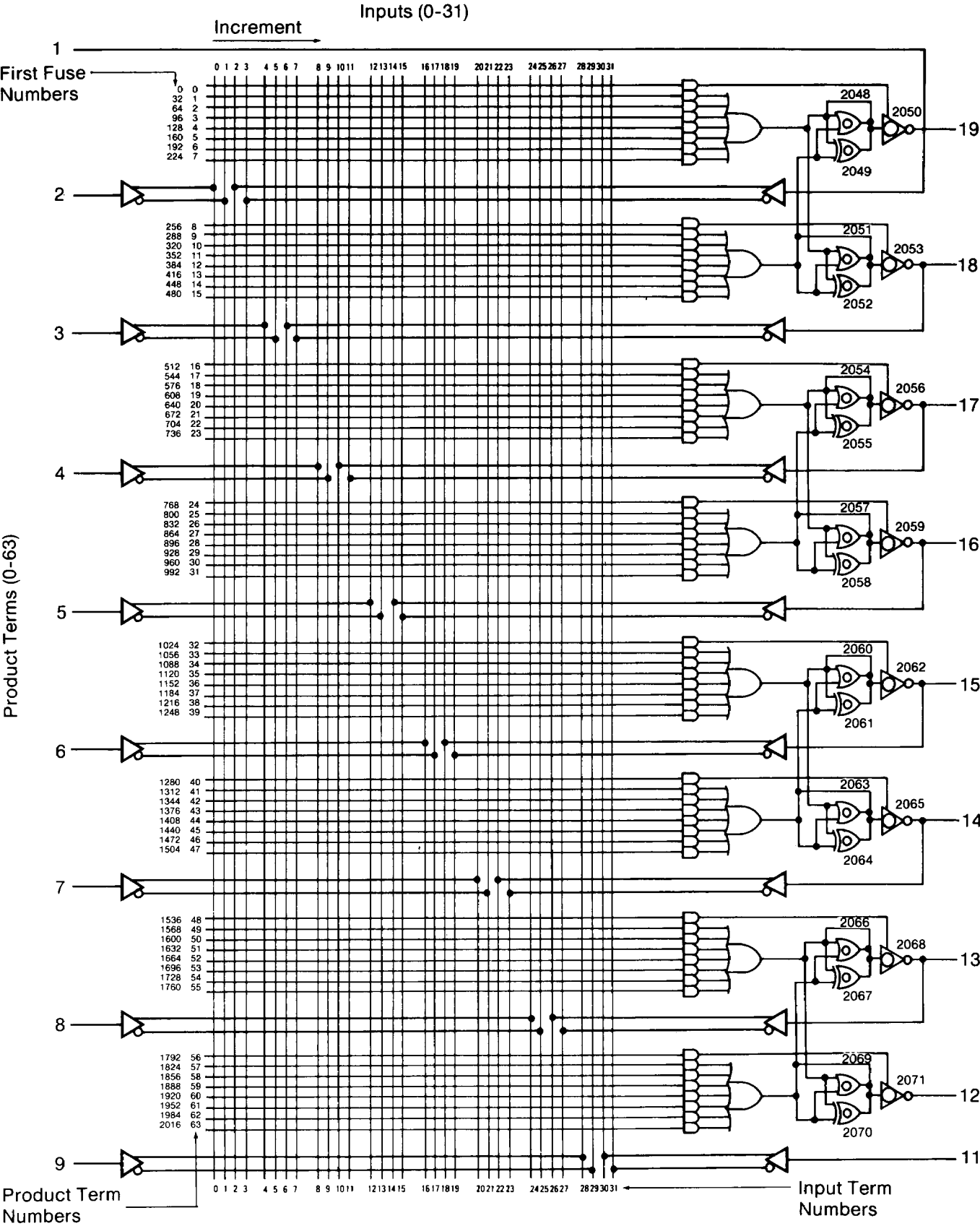
Logic Diagram
EPL14P4A
EPL14P4B



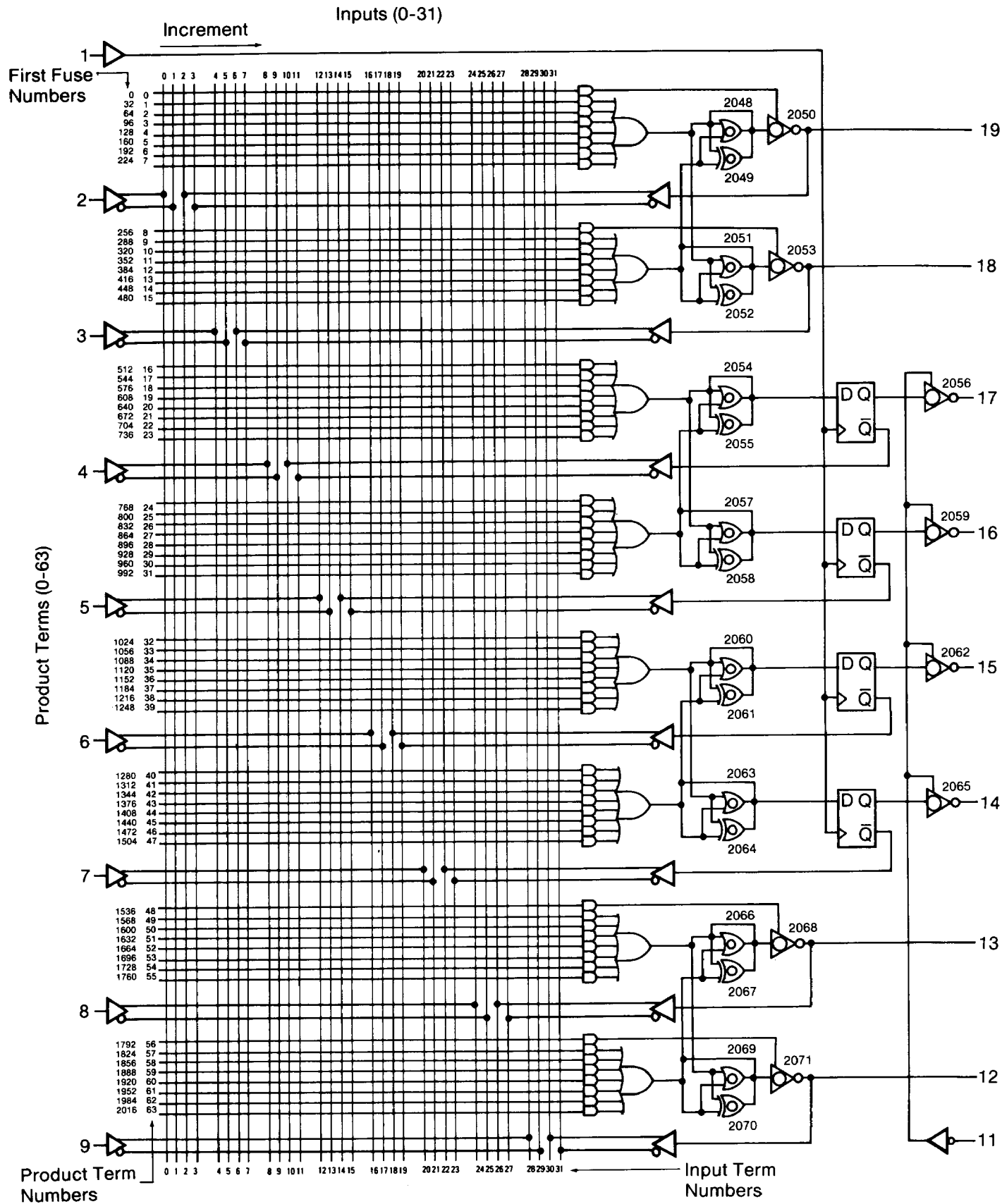
Logic Diagram
 EPL16P2A
 EPL16P2B



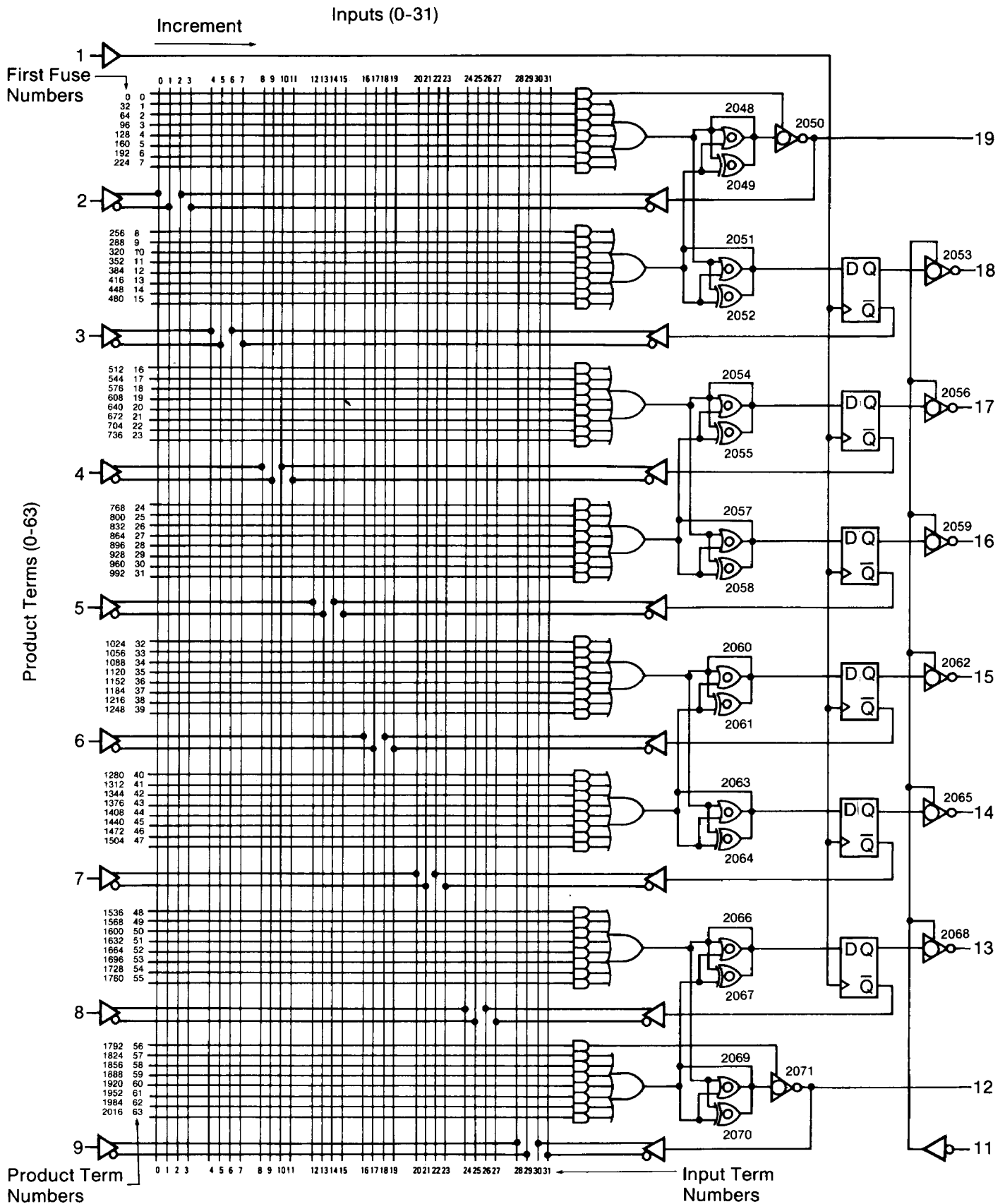
Logic Diagram
EPL16P8B



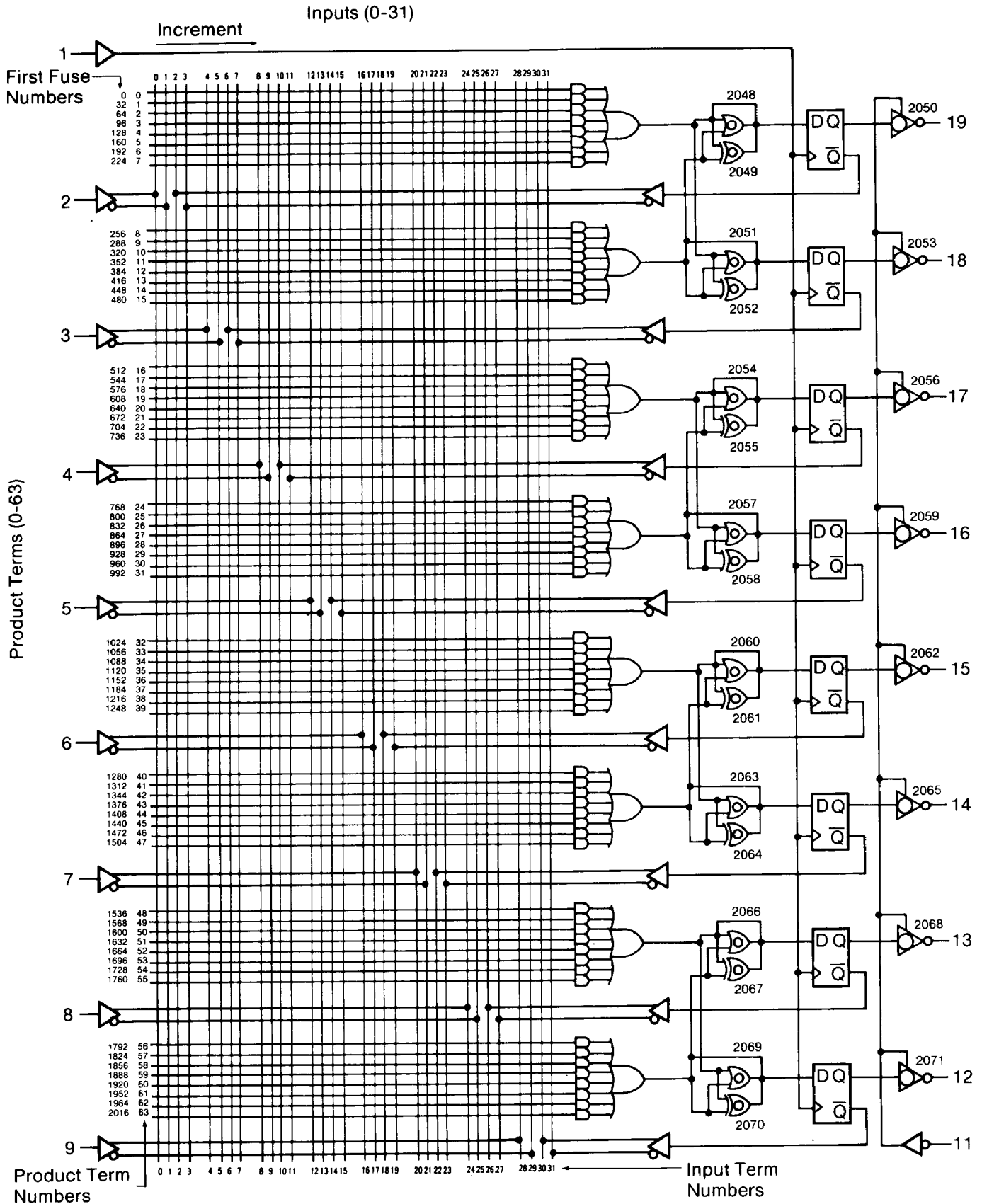
Logic Diagram
EPL16RP4B



Logic Diagram
EPL16RP6B



Logic Diagram
EPL16RP8B



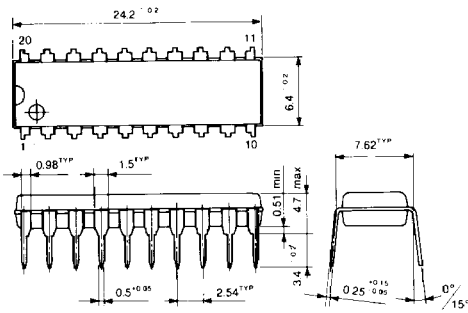
Cross Reference Guide EPL to PAL

| EPL Group I | 10P8 | 12P6 | 14P4 | 16P2 |
|-------------|------|------|------|------|
| Small PAL | 10H8 | 12H6 | 14P4 | 16H2 |
| | 10L8 | 12L6 | 14L4 | 16L2 |
| | 10P8 | 12P6 | 14H4 | 16P2 |
| | | | | 16C1 |

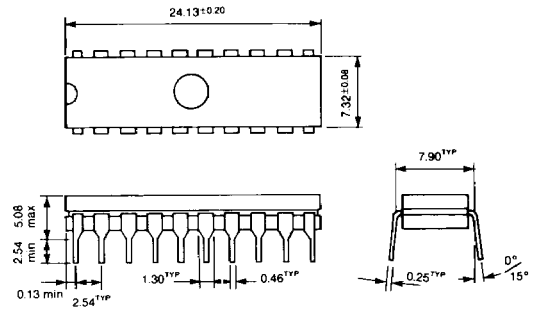
| EPL Group II | 16P8 | 16RP8 | 16RP6 | 16RP4 |
|--------------|------|-------|-------|-------|
| Medium PAL | 16H8 | 16R8 | 16R6 | 16R4 |
| | 16L8 | 16RP8 | 16RP6 | 16RP4 |
| | 16P8 | | | |

Packaging

20-Pin Plastic DIP Packaging 1-Shot (Unit: mm)



20-Pin Ceramic DIP Reprogrammable (Glass Sealed with a quartz window) (Unit: mm)



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